Docket No.: SON-2313
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Satoshi Ikeda

Application No.: 10/052,736 Confirmation No.: 3283

Filed: January 23, 2002 Art Unit: 2138

For: SEMICONDUCTOR TESTING APPARATUS AND METHOD Examiner: J. C. Kerveros

TRANSMITTAL OF APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Transmitted herewith is the Appeal Brief in this application, with respect to the Notice of Appeal filed herewith.

The Office Action of February 7, 2007 *reopened* prosecution prior to a decision on the merits by the Board of Patent Appeals and Interferences. Accordingly, please apply the fee paid on March 30, 2005 for the Appeal Brief. M.P.E.P. §1204.01.

No additional fee to the Patent and Trademark Office for this Appeal Brief is believed to be required. But if any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

Dated: April 12, 2007

Respectfully submitted,

By R. D. 47,255
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In re Patent Application of: Satoshi Ikeda	Confirmation No.: 3283
Application No.: 10/052,736	Art Unit: 2133
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For: SEMICONDUCTOR TESTING APPARATUS AND METHOD	

APPELLANT'S BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

This is an Appeal Brief under 37 C.F.R. §41.37 appealing the final decision of the Examiner dated February 7, 2007. Each of the topics required by 37 C.F.R. §41.37 is presented herewith and is labeled appropriately.

This brief is in furtherance of the Office Action on February 7, 2007.

A Notice of Appeal has been filed in this case concurrent with the Appeal Brief.

I. REAL PARTY IN INTEREST

Sony Corporation of Tokyo, Japan ("Sony") is the real party in interest of the present application. An assignment of all rights in the present application to Sony was executed by the inventor and recorded by the U.S. Patent and Trademark Office at **reel 012531, frame 0679.**

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Thus, the status of the claims is as follows:

Claims 1-5 (canceled);

Claims 6-32 (rejected).

No claims are indicated within the Office Action to contain allowable subject matter.

Accordingly, Appellant hereby appeals the rejection of claims 6-32 which are presented in the Claims Appendix.

IV. STATUS OF AMENDMENTS

Subsequent to the rejection of February 7, 2007, an Amendment in Response to Non-Final Office Action has been filed concurrent with the Appeal Brief for the purpose of cancelling claim 3.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The following description is provided for illustrative purposes and is not intended to limit the scope of the invention.

The present invention relates to an apparatus and a method for testing a semiconductor, and more particularly to those for testing a semiconductor device by first supplying an input signal of a test pattern to the semiconductor device and then comparing the output signal from the semiconductor device with a predetermined expected value.

Claims 6, 10, 15 - Control means 110 is adapted to generate a timing signal and an address specifying signal (specification at page 9, lines 11-16). The duration of said test pattern cycle period can be varied (specification at page 9, lines 16-20). The rate of modification for the address specifying signal is the test pattern cycle period (specification at figures 2, 3A, 3B, 3C, and 4).

The test pattern memory means 130 adapted to store a first test pattern, wherein the first test pattern is outputted from the test pattern memory means in response to an address specifying signal (specification at page 10, lines 10-15). The rate of output for the first test pattern is the test pattern cycle period (specification at page 10, lines 13-15).

Test pattern generation means 120 is adapted to generate an input test pattern signal by combining the first test pattern with the timing signal (specification at page 10, lines 3-7). Moreover, semiconductor device under test 500 receives the input test pattern signal (specification at figure 1).

Claim 7 - Decision means 140 adapted to detect a failure within said semiconductor device by comparing an output test pattern signal received from said semiconductor device under test 500 with said first test pattern (specification at page 11, line 22 to page 12, line 3).

Claim 8 - Claim 8 is drawn to the semiconductor testing apparatus according to claim 6, wherein said control means 110 is adapted to vary said duration of said test pattern cycle period (specification at page 12, lines 17-21).

Claim 9 - Claim 9 is drawn to the semiconductor testing apparatus according to claim 6, wherein said first test pattern is located at an address within said test pattern memory means 130 (specification at page 10, lines 10-15).

Claims 11, 12 - Claim 11 is drawn to the semiconductor testing apparatus according to claim 6, wherein said control means 110 receiving set information to generate said timing signal and said address specifying signal, said set information establishing said duration of said test pattern cycle period (specification at page 9, lines 16-20).

Claim 13 - Claim 13 is drawn to the semiconductor testing apparatus according to claim 11, wherein said test pattern cycle period is narrowed by varying said set information (specification at page 13, line 2 to page 15, line 11).

Claim 14 - Claim 14 is drawn to the semiconductor testing apparatus according to claim 11, wherein said test pattern cycle period is widened by varying said set information (specification at page 15, line 12 to page 16, line 2).

Claim 16 - Claim 16 is drawn to the semiconductor testing apparatus according to claim 15, wherein said duration of said test pattern cycle period only for said first test pattern is narrowed (specification at page 13, line 2 to page 15, line 11).

Claim 17 - Claim 17 is drawn to the semiconductor testing apparatus according to claim 15, wherein said duration of said test pattern cycle period for said first test pattern and for said plurality of test patterns is narrowed (specification at page 13, line 2 to page 15, line 11).

Claim 18 - Claim 18 is drawn to the semiconductor testing apparatus according to claim 15, wherein said duration of said test pattern cycle period for said plurality of test patterns is narrowed successively from the top pattern address throughout the entire test pattern in order (specification at page 13, line 2 to page 15, line 11).

Claim 19 - Claim 19 is drawn to the semiconductor testing apparatus according to claim 15, wherein said duration of said test pattern cycle period only for said first test pattern is widened (specification at page 15, line 12 to page 16, line 2).

Claim 20 - Claim 20 is drawn to the semiconductor testing apparatus according to claim 15, wherein said duration of said test pattern cycle period for said first test pattern and for said plurality of test patterns is widened (specification at page 15, line 12 to page 16, line 2).

Claim 21 - Claim 12 is drawn to the semiconductor testing apparatus according to claim 15, wherein said duration of said test pattern cycle period for said plurality of test patterns

is widened successively from the top pattern address throughout the entire test pattern in order (specification at page 15, line 12 to page 16, line 2).

Claims 22, 26 - Claim 22 is drawn to a semiconductor testing method for conducting a test of a semiconductor device comprising the steps of:

generating a timing signal having a test pattern cycle period (specification at page 9, lines 11-16);

varying the duration of said test pattern cycle period (specification at page 9, lines 16-20);

generating an address specifying signal, the rate of modification for said address specifying signal being said test pattern cycle period (specification at figures 2, 3A, 3B, 3C, and 4);

storing a first test pattern within test pattern memory means 130 (specification at page 10, lines 10-15);

outputting said first test pattern from within test pattern memory means 130 in response to said address specifying signal, the rate of output for said first test pattern being said test pattern cycle period (specification at page 10, lines 10-15);

combining said first test pattern with said timing signal to generate an input test pattern signal, a semiconductor device under test 500 receiving said input test pattern signal (specification at page 10, lines 3-7); and

comparing an output test pattern signal from said semiconductor device under test with said first test pattern (specification at figure 1).

Claim 23 - Claim 23 is drawn to the semiconductor testing method according to claim 22, further comprising the steps of:

receiving set information to generate said timing signal and said address specifying signal (specification at page 9, lines 16-20); and

using said set information to establish said duration of said test pattern cycle period (specification at page 11, lines 13-15).

Claim 24 - Claim 24 is drawn to the semiconductor testing method according to claim 23, wherein said test pattern cycle period is narrowed by varying said set information (specification at page 13, line 2 to page 15, line 11).

Claim 25 - Claim 25 is drawn to the semiconductor testing method according to claim 23, wherein said test pattern cycle period is widened by varying said set information (specification at page 15, line 12 to page 16, line 2).

Claim 27 - Claim 27 is drawn to the semiconductor testing method according to claim 22, wherein said duration of said test pattern cycle period only for said first test pattern is narrowed (specification at page 13, line 2 to page 15, line 11).

Claim 28 - Claim 28 is drawn to the semiconductor testing method according to claim 22, wherein said duration of said test pattern cycle period for said first test pattern and for said plurality of test patterns is narrowed (specification at page 13, line 2 to page 15, line 11).

Claim 29 - Claim 29 is drawn to the semiconductor testing method according to claim 22, wherein said duration of said test pattern cycle period for said plurality of test patterns is narrowed successively from the top pattern address throughout the entire test pattern in order (specification at page 13, line 2 to page 15, line 11).

Claim 30 - Claim 30 is drawn to the semiconductor testing method according to claim 22, wherein said duration of said test pattern cycle period only for said first test pattern is widened (specification at page 15, line 12 to page 16, line 2).

Claim 31 - Claim 31 is drawn to the semiconductor testing method according to claim 22, wherein said duration of said test pattern cycle period for said first test pattern and for said plurality of test patterns is widened (specification at page 15, line 12 to page 16, line 2).

Claim 32 - Claim 32 is drawn to the semiconductor testing method according to claim 22, wherein said duration of said test pattern cycle period for said plurality of test patterns is widened successively from the top pattern address throughout the entire test pattern in order (specification at page 15, line 12 to page 16, line 2).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issues presented for consideration in this appeal are as follows:

Whether the Examiner erred in rejecting claims 3 and 6-32 under 35 U.S.C. §102 as allegedly being anticipated by U.S. Patent No. 6,553,529 Reichert.

This issue will be discussed hereinbelow.

VII. ARGUMENT

In the Office Action of February 7, 2007:

The Examiner erred in rejecting claims 3 and 6-32 under 35 U.S.C. §102 as allegedly being anticipated by U.S. Patent No. 6,553,529 Reichert.

For at least the following reasons, Appellant submits that this rejection is both technically and legally unsound and should therefore be reversed.

The arguments set forth in the following section provide reasons why these claims are considered patentable, 37 C.F.R. §41.37(c)(1)(vii).

The Examiner erred in rejecting claims 3 and 6-32 under 35 U.S.C. §102 as allegedly being anticipated by U.S. Patent No. 6,553,529 Reichert.

This rejection is traversed at least for the following reasons.

Claim 3 - While not conceding the propriety of this rejection and to advance the prosecution of the above-identified application, claim 3 has been canceled in the Amendment in Response to Non-Final Office Action filed concurrent with the Appeal Brief.

Claims 6, 10, 15 - Claim 6 is drawn to a semiconductor testing apparatus comprising:

control means adapted to generate a timing signal and an address specifying signal, said timing signal having a test pattern cycle period, the duration of said test pattern cycle period being variable, the rate of modification for said address specifying signal being said test pattern cycle period;

test pattern memory means adapted to store a first test pattern, said first test pattern being outputted from said test pattern memory means in response to said address specifying signal, the rate of output for said first test pattern being said test pattern cycle period; and

test pattern generation means adapted to generate an input test pattern signal by combining said first test pattern with said timing signal, a semiconductor device under test receiving said input test pattern signal.

Reichert - Reichert arguably teaches a low cost timing system for highly accurate multi-modal semiconductor testing.

Referring more particularly to Figure 2 of Reichert, the timing logic 34 according to one embodiment of the present invention, supports multi-modal testing of high and low-speed DUT pins by selectively providing timing values for assignment to desired user timings (Reichert at Figure 2, column 4, lines 46-50).

Reichert arguably teaches that the timing logic preferably includes a programmable PLL-based master oscillator MOSC 40 and a timing generator 45 that provides respective enable inputs to a plurality of edge generators in the form of respective interpolators EG0-EG12 (Reichert at Figure 2, column 4, lines 50-54).

Associated with each edge generator is a corresponding delay element (not shown) and an enable input supplied by the timing generator 45 (Reichert at Figure 2, column 4, lines 58-60).

The edge generator outputs are fed to a selector circuit that includes respective networks of AND and OR gates (not shown) that collectively define an array of four multiplexers M1-M4 (Reichert at Figure 2, column 5, lines 5-10).

The multiplexers respond to respective static registers 46 that are programmed at set-up time to, during operation, selectively pass timing signals to the drive/compare circuitry 42 (Reichert at Figure 2, column 5, lines 10-13).

However, Reichert fails to disclose, teach, or suggest the timing logic 34 as being adapted to generate a timing signal and an address specifying signal.

The Office Action identifies element 22 of Reichert as a control means (Office Action at page 6). In this regard, Reichert arguably teaches a *computer workstation 22* operating as a test controller (Reichert at Figure 1, column 4, lines 21-22).

In operation, the edge generators EG0-EG12 may be configured to maximize timing resolution and flexibility depending on the expected modes of operation (Reichert at column 5, lines 17-19).

Control of the edge generators is carried out by pre-programming *the test controller 22 and the edgeset memory 36* to fire predetermined edge generators at the specific increments of time following the beginning of the DUT cycle (BOC) (Reichert at column 5, lines 19-23).

For high-speed ports, the edge generator resources are allocated by the user to fire at specific timings designated by the user at very high accuracies (Reichert at column 5, lines 23-26).

The test controller 22 automatically assigns the edge generator closest to the user-programmed timing (in this case for Drive 0, EG0) to fire while maintaining an acceptable level of accuracy (Reichert at column 7, lines 9-12). Each assignment is stored in the edgeset memory as the edge generator number and the number of master oscillator cycles (Reichert at column 7, lines 12-14).

However, Reichert fails to disclose, teach, or suggest the test controller 22 as being adapted to generate a timing signal and an address specifying signal.

- *Thus, Reichert fails to disclose, teach, or suggest control means adapted to generate a timing signal and an address specifying signal, said timing signal having a test pattern cycle period, the duration of said test pattern cycle period being variable, the rate of modification for said address specifying signal being said test pattern cycle period.*

The test controller couples to a system bus 26 for distributing control signals between the test controller and a *pattern generation circuit 24*, a timing system 30, and a failure processing circuit 50 (Reichert at Figure 1, column 4, lines 22-25).

An optional global timing memory circuit or timeset memory 38 couples to the *pattern generation circuit 24* via the global timeset address line 29 and feeds pre-programmed local timing data to the edgeset memory 36 to enable a reduction in the memory capacity thereof (Reichert at Figure 1, column 4, lines 41-45).

However, Reichert fails to disclose, teach, or suggest the pattern generation circuit 24 as being adapted to output a first test pattern in response to an address specifying signal generated by the control means, wherein the rate of output for the first test pattern is the test pattern cycle period.

The Office Action identifies an alleged pattern memory within the computer workstation 22 of Reichert as the test pattern memory means (Office Action at page 6). In this regard, Reichert arguably teaches that control of the edge generators is carried out by pre-programming *the test controller 22 and the edgeset memory 36* to fire predetermined edge generators at the specific increments of time following the beginning of the DUT cycle (BOC) (Reichert at column 5, lines 19-23).

However, Reichert fails to disclose, teach, or suggest the test controller 22 as being adapted to output a first test pattern in response to an address specifying signal generated by the control means, wherein the rate of output for the first test pattern is the test pattern cycle period.

- *Thus, Reichert fails to disclose, teach, or suggest test pattern memory means adapted to store a first test pattern, said first test pattern being outputted from said test pattern memory means in response to said address specifying signal, the rate of output for said first test pattern being said test pattern cycle period.*

Claim 7 - Claim 7 is drawn to the semiconductor testing apparatus according to claim 6, further comprising:

> decision means adapted to detect a failure within said semiconductor device by comparing an output test pattern signal received from said semiconductor device under test with said first test pattern.

Reichert - Reichert arguably teaches the presence of a failure processing circuit 50 (Reichert at Figure 1, column 4, lines 22-25).

As previously noted hereinabove, the Office Action identifies an alleged pattern memory within the computer workstation 22 of Reichert as the test pattern memory means (Office Action at page 6).

A pin data line 27 and a global timeset address line 29 couple the pattern generator to the timing system while pattern information to and from the failure processor is distributed via the system bus 26 (Reichert at Figure 1, column 4, lines 29-34).

However, Reichert fails to disclose, teach, or suggest the failure processing circuit 50 as being adapted to detect a failure within the DUT 28 by comparing an output test pattern signal received from the DUT with the first test pattern outputted from the alleged test pattern memory means.

Claim 8 - Claim 8 is drawn to the semiconductor testing apparatus according to claim 6, wherein said control means is adapted to vary said duration of said test pattern cycle period.

Reichert - As noted hereinabove, the Office Action identifies element 22 of Reichert as a control means (Office Action at page 6). In this regard, Reichert arguably teaches a *computer workstation 22* operating as a test controller (Reichert at Figure 1, column 4, lines 21-22).

However, Reichert fails to disclose, teach, or suggest the computer workstation 22 as being adapted to vary said duration of said test pattern cycle period.

Claim 9 - Claim 9 is drawn to the semiconductor testing apparatus according to claim 6, wherein said first test pattern is located at an address within said test pattern memory means.

Reichert - As noted hereinabove, the Office Action identifies an alleged pattern memory within the computer workstation 22 of Reichert as the test pattern memory means (Office Action at page 6).

However, Reichert is silent regarding the first test pattern being located at an address within the test pattern memory means.

Claims 11, 12 - Claim 11 is drawn to the semiconductor testing apparatus according to claim 6, wherein said control means receiving set information to generate said timing signal and said address specifying signal, said set information establishing said duration of said test pattern cycle period.

Reichert - As noted hereinabove, the Office Action identifies element 22 of Reichert as a control means (Office Action at page 6). In this regard, Reichert arguably teaches a *computer workstation 22* operating as a test controller (Reichert at Figure 1, column 4, lines 21-22).

However, Reichert fails to disclose, teach, or suggest the test controller 22 as being adapted to generate a timing signal and an address specifying signal.

Claim 13 - Claim 13 is drawn to the semiconductor testing apparatus according to claim 11, wherein said test pattern cycle period is narrowed by varying said set information.

Reichert - Reichert is **silent** as to whether or not a test pattern cycle period is narrowed by varying set information.

Claim 14 - Claim 14 is drawn to the semiconductor testing apparatus according to claim 11, wherein said test pattern cycle period is widened by varying said set information.

Reichert - Reichert is **silent** as to whether or not a test pattern cycle period is widened by varying set information.

Claim 16 - Claim 16 is drawn to the semiconductor testing apparatus according to claim 15, wherein said duration of said test pattern cycle period only for said first test pattern is narrowed.

Reichert - Reichert is **silent** as to whether or not the duration of the test pattern cycle period only for the first test pattern is narrowed.

Claim 17 - Claim 17 is drawn to the semiconductor testing apparatus according to claim 15, wherein said duration of said test pattern cycle period for said first test pattern and for said plurality of test patterns is narrowed.

Reichert - Reichert is **silent** as to whether or not the duration of the test pattern cycle period for the first test pattern and for the plurality of test patterns is narrowed.

Claim 18 - Claim 18 is drawn to the semiconductor testing apparatus according to claim 15, wherein said duration of said test pattern cycle period for said plurality of test patterns is narrowed successively from the top pattern address throughout the entire test pattern in order.

Reichert - Reichert is **silent** as to whether or not the duration of said test pattern cycle period for said plurality of test patterns is narrowed successively from the top pattern address throughout the entire test pattern in order.

Claim 19 - Claim 19 is drawn to the semiconductor testing apparatus according to claim 15, wherein said duration of said test pattern cycle period only for said first test pattern is widened.

Reichert - Reichert is **silent** as to whether or not the duration of the test pattern cycle period only for the first test pattern is widened.

Claim 20 - Claim 20 is drawn to the semiconductor testing apparatus according to claim 15, wherein said duration of said test pattern cycle period for said first test pattern and for said plurality of test patterns is widened.

Reichert - Reichert is **silent** as to whether or not the duration of said test pattern cycle period for the first test pattern and for the plurality of test patterns is widened.

Claim 21 - Claim 12 is drawn to the semiconductor testing apparatus according to claim 15, wherein said duration of said test pattern cycle period for said plurality of test patterns is widened successively from the top pattern address throughout the entire test pattern in order.

Reichert - Reichert is **silent** as to whether or not the duration of said test pattern cycle period for said plurality of test patterns is widened successively from the top pattern address throughout the entire test pattern in order.

Claims 22, 26 - Claim 22 is drawn to a semiconductor testing method for conducting a test of a semiconductor device comprising the steps of:

generating a timing signal having a test pattern cycle period;

varying the duration of said test pattern cycle period;

generating an address specifying signal, the rate of modification for said address specifying signal being said test pattern cycle period;

storing a first test pattern within test pattern memory means;

outputting said first test pattern from within test pattern memory means in response to said address specifying signal, the rate of output for said first test pattern being said test pattern cycle period;

combining said first test pattern with said timing signal to generate an input test pattern signal, a semiconductor device under test receiving said input test pattern signal; and

comparing an output test pattern signal from said semiconductor device under test with said first test pattern.

Reichert - Reichert arguably teaches a low cost timing system for highly accurate multi-modal semiconductor testing.

Referring more particularly to Figure 2 of Reichert, the timing logic 34 according to one embodiment of the present invention, supports multi-modal testing of high and low-speed

DUT pins by selectively providing timing values for assignment to desired user timings (Reichert at Figure 2, column 4, lines 46-50).

Reichert arguably teaches that the timing logic preferably includes a programmable PLL-based master oscillator MOSC 40 and a timing generator 45 that provides respective enable inputs to a plurality of edge generators in the form of respective interpolators EG0-EG12 (Reichert at Figure 2, column 4, lines 50-54).

Associated with each edge generator is a corresponding delay element (not shown) and an enable input supplied by the timing generator 45 (Reichert at Figure 2, column 4, lines 58-60).

The edge generator outputs are fed to a selector circuit that includes respective networks of AND and OR gates (not shown) that collectively define an array of four multiplexers M1-M4 (Reichert at Figure 2, column 5, lines 5-10).

The multiplexers respond to respective static registers 46 that are programmed at set-up time to, during operation, selectively pass timing signals to the drive/compare circuitry 42 (Reichert at Figure 2, column 5, lines 10-13).

However, Reichert is silent as to the presence or absence of an address specifying signal.

The Office Action identifies element 22 of Reichert as a control means (Office Action at page 6). In this regard, Reichert arguably teaches a *computer workstation 22* operating as a test controller (Reichert at Figure 1, column 4, lines 21-22).

In operation, the edge generators EG0-EG12 may be configured to maximize timing resolution and flexibility depending on the expected modes of operation (Reichert at column 5, lines 17-19).

Control of the edge generators is carried out by pre-programming *the test controller 22 and the edgeset memory 36* to fire predetermined edge generators at the specific increments of time following the beginning of the DUT cycle (BOC) (Reichert at column 5, lines 19-23).

For high-speed ports, the edge generator resources are allocated by the user to fire at specific timings designated by the user at very high accuracies (Reichert at column 5, lines 23-26).

The test controller 22 automatically assigns the edge generator closest to the user-programmed timing (in this case for Drive 0, EG0) to fire while maintaining an acceptable level of accuracy (Reichert at column 7, lines 9-12). Each assignment is stored in the edgeset memory as the edge generator number and the number of master oscillator cycles (Reichert at column 7, lines 12-14).

However, Reichert fails to disclose, teach, or suggest the test controller 22 as being adapted to generate a timing signal and an address specifying signal.

- *Thus, Reichert fails to disclose, teach, or suggest generating an address specifying signal, the rate of modification for said address specifying signal being said test pattern cycle period.*

The test controller couples to a system bus 26 for distributing control signals between the test controller and a *pattern generation circuit 24*, a timing system 30, and a failure processing circuit 50 (Reichert at Figure 1, column 4, lines 22-25).

An optional global timing memory circuit or timeset memory 38 couples to the *pattern generation circuit 24* via the global timeset address line 29 and feeds pre-programmed local timing data to the edgeset memory 36 to enable a reduction in the memory capacity thereof (Reichert at Figure 1, column 4, lines 41-45).

However, Reichert fails to disclose, teach, or suggest the pattern generation circuit 24 as being adapted to output a first test pattern in response to an address specifying signal generated by the control means, wherein the rate of output for the first test pattern is the test pattern cycle period.

The Office Action identifies an alleged pattern memory within the computer workstation 22 of Reichert as the test pattern memory means (Office Action at page 6). In this

regard, Reichert arguably teaches that control of the edge generators is carried out by pre-programming *the test controller 22 and the edgeset memory 36* to fire predetermined edge generators at the specific increments of time following the beginning of the DUT cycle (BOC) (Reichert at column 5, lines 19-23).

However, Reichert fails to disclose, teach, or suggest the test controller 22 as being adapted to output a first test pattern in response to an address specifying signal generated by the control means, wherein the rate of output for the first test pattern is the test pattern cycle period.

- *Thus, Reichert fails to disclose, teach, or suggest outputting said first test pattern from within test pattern memory means in response to said address specifying signal, the rate of output for said first test pattern being said test pattern cycle period.*

Claim 23 - Claim 23 is drawn to the semiconductor testing method according to claim 22, further comprising the steps of:

receiving set information to generate said timing signal and said address specifying signal; and

using said set information to establish said duration of said test pattern cycle period.

Reichert - Reichert is **silent** as to a step of receiving set information to generate the timing signal and the address specifying signal.

Reichert - Reichert is **silent** as to a step of using the set information to establish the duration of the test pattern cycle period.

Claim 24 - Claim 24 is drawn to the semiconductor testing method according to claim 23, wherein said test pattern cycle period is narrowed by varying said set information.

Reichert - Reichert is **silent** as to whether or not the test pattern cycle period is narrowed by varying the set information.

Claim 25 - Claim 25 is drawn to the semiconductor testing method according to claim 23, wherein said test pattern cycle period is widened by varying said set information.

Reichert - Reichert is **silent** as to whether or not the test pattern cycle period is widened by varying the set information.

Claim 27 - Claim 27 is drawn to the semiconductor testing method according to claim 22, wherein said duration of said test pattern cycle period only for said first test pattern is narrowed.

Reichert - Reichert is **silent** as to whether or not the duration of the test pattern cycle period only for the first test pattern is narrowed.

Claim 28 - Claim 28 is drawn to the semiconductor testing method according to claim 22, wherein said duration of said test pattern cycle period for said first test pattern and for said plurality of test patterns is narrowed.

Reichert - Reichert is **silent** as to whether or not the duration of the test pattern cycle period for the first test pattern and for the plurality of test patterns is narrowed.

Claim 29 - Claim 29 is drawn to the semiconductor testing method according to claim 22, wherein said duration of said test pattern cycle period for said plurality of test patterns is narrowed successively from the top pattern address throughout the entire test pattern in order.

Reichert - Reichert is **silent** as to whether or not the duration of the test pattern cycle period for the plurality of test patterns is narrowed successively from the top pattern address throughout the entire test pattern in order.

Claim 30 - Claim 30 is drawn to the semiconductor testing method according to claim 22, wherein said duration of said test pattern cycle period only for said first test pattern is widened.

Reichert - Reichert is **silent** as to whether or not the duration of the test pattern cycle period only for the first test pattern is widened.

Claim 31 - Claim 31 is drawn to the semiconductor testing method according to claim 22, wherein said duration of said test pattern cycle period for said first test pattern and for said plurality of test patterns is widened.

Reichert - Reichert is **silent** as to whether or not the duration of the test pattern cycle period for the first test pattern and for the plurality of test patterns is widened.

Claim 32 - Claim 32 is drawn to the semiconductor testing method according to claim 22, wherein said duration of said test pattern cycle period for said plurality of test patterns is widened successively from the top pattern address throughout the entire test pattern in order.

Reichert - Reichert is **silent** as to whether or not the duration of the test pattern cycle period for the plurality of test patterns is widened successively from the top pattern address throughout the entire test pattern in order.

Conclusion

The claims are considered allowable for the same reasons discussed above, as well as for the additional features they recite. Reversal of the Examiner's decision is respectfully requested.

Dated: April 12, 2007

Respectfully submitted,

By _____

Ronald P. Kananen
Registration No.: 24,104
RADER, FISHMAN & GRAUER PLLC
Correspondence Customer Number: 23353
Attorney for Applicant

CLAIMS APPENDIX

1-5. (Canceled)

6. (Previously presented) A semiconductor testing apparatus comprising:

control means adapted to generate a timing signal and an address specifying signal, said timing signal having a test pattern cycle period, the duration of said test pattern cycle period being variable, the rate of modification for said address specifying signal being said test pattern cycle period;

test pattern memory means adapted to store a first test pattern, said first test pattern being outputted from said test pattern memory means in response to said address specifying signal, the rate of output for said first test pattern being said test pattern cycle period; and

test pattern generation means adapted to generate an input test pattern signal by combining said first test pattern with said timing signal, a semiconductor device under test receiving said input test pattern signal.

7. (Previously presented) The semiconductor testing apparatus according to claim 6, further comprising:

decision means adapted to detect a failure within said semiconductor device by comparing an output test pattern signal received from said semiconductor device under test with said first test pattern.

8. (Previously presented) The semiconductor testing apparatus according to claim 6, wherein said control means is adapted to vary said duration of said test pattern cycle period.

9. (Previously presented) The semiconductor testing apparatus according to claim 6, wherein said first test pattern is located at an address within said test pattern memory means.

10. (Previously presented) The semiconductor testing apparatus according to claim 6, wherein said semiconductor device is tested during said test pattern cycle period.

11. (Previously presented) The semiconductor testing apparatus according to claim 6, wherein said control means receiving set information to generate said timing signal and said address specifying signal, said set information establishing said duration of said test pattern cycle period.

12. (Previously presented) The semiconductor testing apparatus according to claim 11, wherein said control means controls the timing of generation of said first test pattern on the basis of said set information.

13. (Previously presented) The semiconductor testing apparatus according to claim 11, wherein said test pattern cycle period is narrowed by varying said set information.

14. (Previously presented) The semiconductor testing apparatus according to claim 11, wherein said test pattern cycle period is widened by varying said set information.

15. (Previously presented) The semiconductor testing apparatus according to claim 6, wherein said test pattern memory means stores a plurality of test patterns, said plurality of test patterns being outputted from said test pattern memory means in response to said address specifying signal, the rate of output for said plurality of test patterns being said test pattern cycle period.

16. (Previously presented) The semiconductor testing apparatus according to claim 15, wherein said duration of said test pattern cycle period only for said first test pattern is narrowed.

17. (Previously presented) The semiconductor testing apparatus according to claim 15, wherein said duration of said test pattern cycle period for said first test pattern and for said plurality of test patterns is narrowed.

18. (Previously presented) The semiconductor testing apparatus according to claim 15, wherein said duration of said test pattern cycle period for said plurality of test patterns is narrowed successively from the top pattern address throughout the entire test pattern in order.

19. (Previously presented) The semiconductor testing apparatus according to claim 15, wherein said duration of said test pattern cycle period only for said first test pattern is widened.

20. (Previously presented) The semiconductor testing apparatus according to claim 15, wherein said duration of said test pattern cycle period for said first test pattern and for said plurality of test patterns is widened.

21. (Previously presented) The semiconductor testing apparatus according to claim 15, wherein said duration of said test pattern cycle period for said plurality of test patterns is widened successively from the top pattern address throughout the entire test pattern in order.

22. (Previously presented) A semiconductor testing method for conducting a test of a semiconductor device comprising the steps of:

generating a timing signal having a test pattern cycle period;

varying the duration of said test pattern cycle period;

generating an address specifying signal, the rate of modification for said address specifying signal being said test pattern cycle period;

storing a first test pattern within test pattern memory means;

outputting said first test pattern from within test pattern memory means in response to said address specifying signal, the rate of output for said first test pattern being said test pattern cycle period;

combining said first test pattern with said timing signal to generate an input test pattern signal, a semiconductor device under test receiving said input test pattern signal; and

comparing an output test pattern signal from said semiconductor device under test with said first test pattern.

23. (Previously presented) The semiconductor testing method according to claim 22, further comprising the steps of:

receiving set information to generate said timing signal and said address specifying signal; and

using said set information to establish said duration of said test pattern cycle period.

24. (Previously presented) The semiconductor testing method according to claim 23, wherein said test pattern cycle period is narrowed by varying said set information.

25. (Previously presented) The semiconductor testing method according to claim 23, wherein said test pattern cycle period is widened by varying said set information.

26. (Previously presented) The semiconductor testing method according to claim 22, wherein said test pattern memory means stores a plurality of test patterns, said plurality of test patterns being outputted from said test pattern memory means in response to said address specifying signal, the rate of output for said plurality of test patterns being said test pattern cycle period.

27. (Previously presented) The semiconductor testing method according to claim 22, wherein said duration of said test pattern cycle period only for said first test pattern is narrowed.

28. (Previously presented) The semiconductor testing method according to claim 22, wherein said duration of said test pattern cycle period for said first test pattern and for said plurality of test patterns is narrowed.

29. (Previously presented) The semiconductor testing method according to claim 22, wherein said duration of said test pattern cycle period for said plurality of test patterns is narrowed successively from the top pattern address throughout the entire test pattern in order.

30. (Previously presented) The semiconductor testing method according to claim 22, wherein said duration of said test pattern cycle period only for said first test pattern is widened.

31. (Previously presented) The semiconductor testing method according to claim 22, wherein said duration of said test pattern cycle period for said first test pattern and for said plurality of test patterns is widened.

32. (Previously presented) The semiconductor testing method according to claim 22, wherein said duration of said test pattern cycle period for said plurality of test patterns is widened successively from the top pattern address throughout the entire test pattern in order.

EVIDENCE APPENDIX

There is no other evidence which will directly affect or have a bearing on the Board's decision in this appeal.

RELATED PROCEEDINGS APPENDIX

There are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.